2008

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Yang, T.; Liu, Y.; Ye, P. D.; Xuan, Y.; Pal, H.; and Lundstrom, Mark S., "Inversion capacitance-voltage studies on GaAs metal-oxide-semiconductor structure using transparent conducting oxide as metal gate" (2008). *Department of Electrical and Computer Engineering Faculty Publications.* Paper 132.
http://dx.doi.org/10.1063/1.2953080

Inversion capacitance-voltage studies on GaAs metal-oxide-semiconductor structure using transparent conducting oxide as metal gate

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(Received 15 April 2008; accepted 10 June 2008; published online 27 June 2008)

A systematic capacitance-voltage (*C-V*) study has been performed on GaAs metal-oxide-semiconductor (MOS) structures with atomic-layer-deposited Al_2O_3 as gate dielectrics and indium tin oxide (ITO) as the metal gate. The transparent conducting ITO gate allows homogeneous photoillumination on the whole MOS capacitance area, such that one can easily observe the low-frequency (LF) *C-V* and quasistatic *C-V* of GaAs at room temperature. The semiconductor capacitance effect on GaAs MOS devices has also been identified and insightfully discussed based on the obtained LF *C-V* curves. The semiconductor capacitance effect becomes more important for devices with high-mobility channel materials and aggressively scaled high-*k* gate dielectrics.
 [DOI: 10.1063/1.2953080]

Silicon-based complementary metal-oxide-semiconductor (CMOS) devices with traditional structures are approaching fundamental physical limits. Researchers are looking for ways to continue the trend of scaling by using alternative materials and structures that could outperform Si-based CMOS. GaAs is of great interest as an alternative channel material due to its high electron mobility, high saturation velocity, and high bandgap. Although many publications exist in the literature, complete understanding of GaAs metal-oxide-semiconductor (MOS) structures is still limited due to the lack of low-defective, thermodynamically stable dielectrics on GaAs.[1] Using atomic-layer-deposition (ALD) technology, we have successfully integrated ALD high-*k* dielectrics on III-V compound semiconductors and have demonstrated some high-performance MOS devices.[2–4] ALD high-*k*/GaAs MOS structures enables us to explore the inversion characteristics and the semiconductor capacitance effect, which have often been hindered in previous *C-V* studies due to the inferior interface quality or thick oxide.

The major objective of GaAs MOS device research is to realize high-performance enhancement-mode surface channel devices with scalable gate dielectrics.[5–9] The low-frequency (LF) or quasistatic (QS) *C-V* curve is useful to analyze the properties of GaAs MOS structures, such as interface trap density, inversion charge, etc. However, it is difficult to observe LF or QS *C-V* on GaAs MOS device under normal conditions (room temperature and in dark). According to the Shockley–Read–Hall statistics and the low intrinsic carrier concentration (n_i) of GaAs ($n_i = 10^6/\mathrm{cm}^3$), the expected ac frequency to observe LF *C-V* in dark and at room temperature is very low ($\sim$0.002 Hz).[10] For QS *C-V*, the required gate leakage current should be much less than the displacement current. This condition is hard to fulfill for high-*k* dielectrics that are only a few nanometers thick. Three alternative approaches[11] to study LF *C-V* on GaAs are (i) inversion-type MOS field-effect transistors with implanted source and drain, where minority carriers can be injected into the surface channel; (ii) elevated temperature to increase the generation-recombination rates of minority carriers in GaAs; and (iii) photoillumination to increase the minority carrier concentration. However, for a conventional, few hundreds of nanometer thick metal gate (i.e., Ni/Au or Ti/Au on GaAs), the gate is opaque to the light. Under photoillumination, only the edge and a small area within a diffusion length can be illuminated by photons. The large central area, typically tens to hundreds of microns, remains in the dark. In most of cases, no LF *C-V* is observed on GaAs even under illumination measured at 1 KHz–1 MHz.[12] In this letter, we report on using transparent conducting indium tin oxide (ITO) as metal gate for GaAs MOS structure and demonstrate clear LF *C-V* under photoillumination at room temperature and at conventional measurement frequencies. By studying QS *C-V* in dark, the semiconductor capacitance effect on GaAs MOS devices has also been observed and insightfully discussed.

MOS capacitors were fabricated on a 2 in. *n*-type or *p*-type GaAs substrates with substrate doping densities of $5\times10^{17}/\mathrm{cm}^3$. After a NH_4OH based surface pretreatment,[12] 4, 8, 12, 16, and 20 nm ALD Al_2O_3 layers were deposited at 300 °C using an ASM F-120 ALD module. Here, Al_2O_3 was deposited using trimethyl aluminum and water. Postdeposition annealing was then conducted at 600 °C by rapid thermal annealing in N_2 ambient for 30 s. After that, ITO was electron-beam evaporated as the gate electrodes using a shadow mask to avoid extra gate leakage current introduced by process steps with photoresist. ITO is a mixture of indium oxide (In_2O_3) and tin oxide (SnO_2), typically 90% In_2O_3, 10% SnO_2 by weight. It is transparent and colorless in thin layers. The main feature of this material is the combination of electrical conductivity and optical transparency so that it can be used as a transparent gate for GaAs MOS capacitors. When light is on, the whole gate area is illuminated by photons, in contrast to only a small edge area that can be illuminated when conventional metals are used. Electrical contact to the GaAs substrates was made via an electron-beam evaporated Au back gate. The high frequency capacitance was measured using an HP4284A precision *LCR* meter with frequencies varying from 1 KHz to 1 MHz, and QS capacitance was also measured by Keithley595 QS CV meter in this work.

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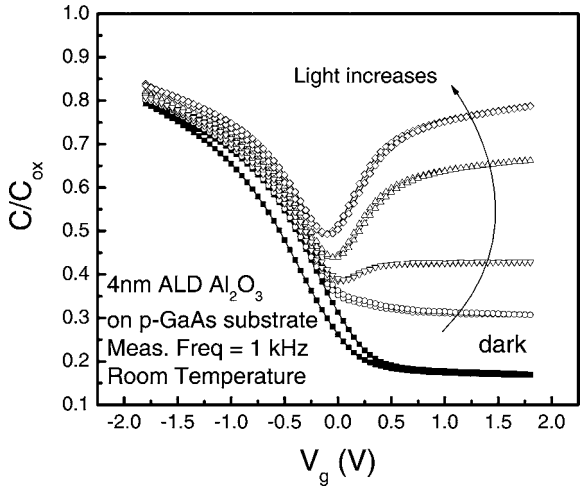

FIG. 1. *C-V* loops on *p*-type GaAs MOS with ITO gate as gradually increasing light illumination measured at 1 kHz. The thickness of oxide is 4 nm. The data are normalized by calculated C_{ox} of 531 pF using capacitance area of 3×10^4 μm^2 and dielectric constant of 8.0. The typical carrier concentration of ITO films is $(2-4)\times10^{20}$/cm^3 in this work (Ref. 22), which is about three orders of magnitude larger than the doping concentration of GaAs. The effect of ITO depletion is not considered on the data analysis.

C-V hysteresis loops of an ITO gate MOS device are shown in Fig. 1(a). This device has a dielectric layer of 4 nm Al_2O_3 on *p*-type GaAs substrate. As shown in the figure, the *C-V* loop still shows high frequency *C-V* characteristic in the dark. However, as light is shone on the device by controlling the input current of the power supply thus light intensity of the microscope lamp, the electron inversion side capacitance increases. LF *C-V* characteristics can be clearly observed when the lamp is fully on. Although the hysteresis of the *C-V* loop in the dark is ~200 mV for this device, the LF *C-V* loops under photoillumination display negligible hysteresis. Photoillumination generates large number of electron-hole pairs in the depletion layer so that the minority concentration (electrons) in GaAs is significantly increased. The carrier generation time becomes much shorter also under photoillumination, therefore the carriers are much easier to catch up with the relatively high frequency ac signals, showing LF *C-V* characteristics.

The light-induced minority carrier concentration and its response time for thermal generation recombination could play more important roles on inversion feature than the interface trap density in the *C-V* measurement. The observed LF or inversion feature in *C-V* measurement is still not a very clear conclusive evidence for Fermi-level unpinning on GaAs. A good exercise is to integrate LF capacitance and obtain the $\psi_s - V$ relationship, a method first developed by Berglund in 1966.[13] The surface potential change on GaAs in Fig. 1 can be calculated to be as large as 1.1 eV, which is comparable to the GaAs bandgap itself. Refined QS *C-V* measurements are also carried out on the similar GaAs MOS structures (not shown), where ψ_s of 1.2 eV is obtained.[14] This is the convincing experimental evidence that the Fermi level at ALD Al_2O_3/GaAs interface moves across nearly the whole bandgap of GaAs and it is not pinned at the midgap. The results on *n*-type GaAs MOS devices show similar characteristics that LF *C-V* is also easily observed under photoillumination. However, if comparing the inversion *C-V* characteristics on *p*-type substrate with that on *n*-type substrate, the hole accumulation on *p*-GaAs or hole inversion on *n*-GaAs always has higher capacitance value than the electron inversion on *p*-GaAs or electron accumulation on *n*-GaAs. This effect is even clearer in the QS *C-V* curves.[5]

To further study the LF *C-V* characteristics in equilibrium situations, QS *C-V* measurements are carried out in dark. Figures 2(a) and 2(b) show the QS *C-V* on *n*- and *p*-type GaAs substrate, respectively, with 16 nm Al_2O_3 as dielectric. From all the LF *C-V* characteristics presented, one can find that the capacitance value is carrier type dependent: hole shows higher capacitance value than electron. This is also confirmed by the self-consistent, Schroedinger–Poisson *C-V* simulations, as shown in Figs. 2(c) and 2(d). (These simulations were done with an effective mass level description of the bandstructure, but very simillar results were obtained with an $sp^3s^*d^5$ tight binding model.[15,16]) Comparison

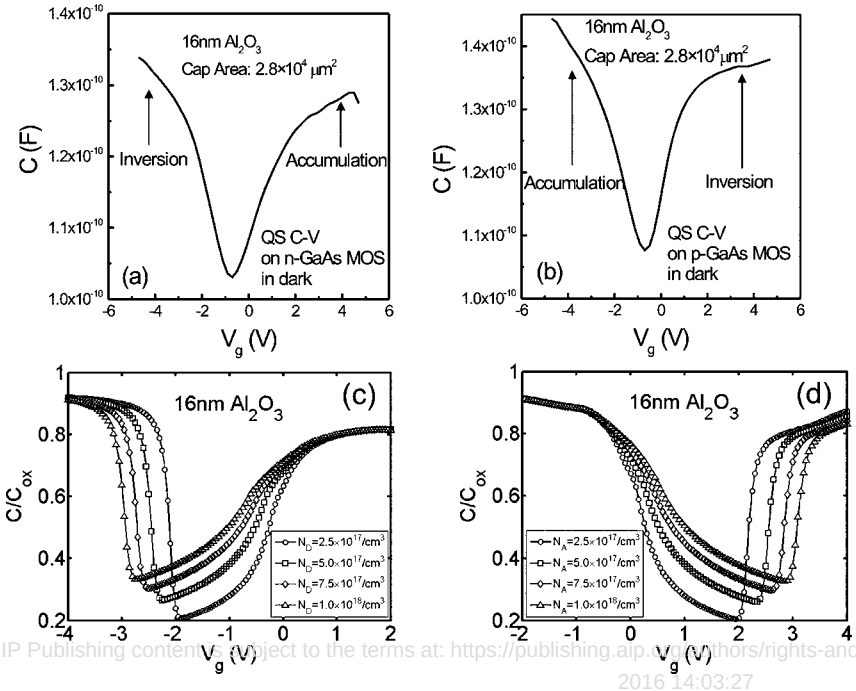

FIG. 2. [(a) and (b)] QS *C-V* characteristics on *n*- and *p*-type GaAs substrates. The thickness of oxide is 16 nm. All measurements are performed in dark with the delay time of 1 s and sweeping rate of ~20 mV/s. The accumulation capacitance value in *p*-type GaAs is expected to be little larger than that in *n*-type GaAs (Ref. 20). [(c) and (d)] Effective mass simulation on *n*- and *p*-type GaAs substrates with different doping concentrations, ITO work function of 4.3 eV, and *zero* interface trap density.

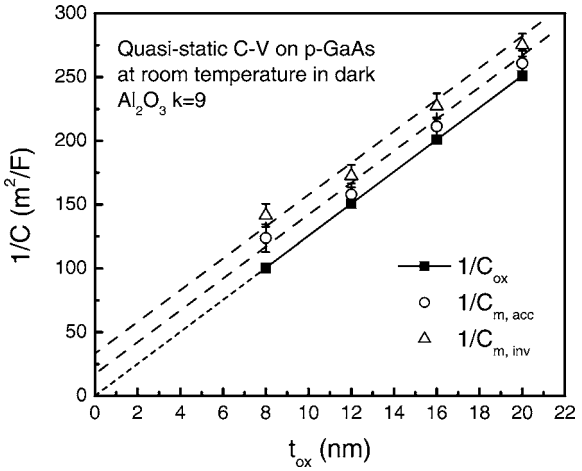

FIG. 3. Measured QS capacitance at accumulation and inversion bias regions as different dielectric thickness on *p*-type GaAs substrate. The error bars are introduced due to the nonasymptotic values in the inversion and accumulation capacitances.

of Figs. 2(c) and 2(d) to the measured results in Figs. 2(a) and 2(b) shows that the simulations are consistent with the experimentally observed higher hole accumulation/inversion layer capacitances as compared to that for electrons.

In a standard MOS capacitor, the oxide capacitance (C_{ox}) and the semiconductor capacitance (C_s) form a series combination which becomes the total capacitance of the gate C_G, yielding $1/C_G=1/C_{ox}+1/C_s$. The semiconductor capacitance is defined as $C_s=-dQ_s/d\psi_s$, where Q_s is the charge in the semiconductor. Although C_s is a routine correction in Si/SiO_2 MOS,[17] less attention is paid to C_s of GaAs MOS due to the inferior interface quality or thick oxide.[5] However, C_s would have significant effect on the C_G on high-mobility III-V channel materials due to their smaller effective mass and lower density of states.[18,19] The fact is that the effective mass of electrons is much smaller than that of holes in GaAs. This explains why measured C_G has a smaller value at electron accumulation (inversion) side than the value obtained from hole inversion (accumulation) side. For a *p*-type GaAs substrate, measured accumulation capacitance value can be expressed by $1/C_{m,acc}=1/C_{ox}+1/(C_{s,acc}+C_{it,acc})$, where $C_{s,acc}$ is the C_s at hole accumulation and $C_{it,acc}$ is the capacitance induced by interface trap under accumulation. Similarly the measured inversion capacitance value can be expressed by $1/C_{m,inv}=1/C_{ox}+1/(C_{s,inv}+C_{it,inv})$, where $C_{s,inv}$ is the C_s at electron inversion, and $C_{it,inv}$ is the interface capacitance under inversion. $C_{it,acc}$ or $C_{it,inv}$ is not the dominant term in this work. Otherwise, there should be no pronounced capacitance lowering from C_{ox}. The widely observed "N-dispersion" effect verifies that $C_{it,acc}<C_{it,inv}$ in *p*-type GaAs,[20] which leads to $1/C_{m,inv}>1/C_{m,acc}$ and it is a different trend from the experimental observation. All of these lead us to conclude that the difference between measured $C_{m,acc}$ and $C_{m,inv}$ is mainly due to the difference between electron and hole semiconductor capacitance.[21]

Figure 3 summarizes measured $1/C_{m,acc}$ and $1/C_{m,inv}$ on *p*-type GaAs substrate versus different dielectric thickness t_{ox}. Assuming that the ideal dielectric constant of Al_2O_3 is 9, the solid line shows the ideal $1/C_{ox}$ curve, which can be extrapolated to be zero as $t_{ox}\rightarrow 0$. The difference between $1/C_{m0,acc}$ and $1/C_{m0,inv}$, the intercepts on the *y*-axis of $1/C_{m,acc}$ and $1/C_{m,inv}$, implies the difference in hole and electron induced in semiconductor capacitance, not considering the possible formation of interface dielectric (similar to SiO_x in Si/high-*k*). For example, $1/C_{m,inv}=225\ m^2/F$ for 16 nm Al_2O_3/p-GaAs leads to $C_{ox}=0.0050\ F/m^2$, $C_s=0.0413\ F/m^2$, and $C_s/C_{ox}=8.26$ for the experiment. This is very close to the simulation value of $C_s/C_{ox}=7.06$.

In summary, a transparent conducting material, ITO, has been used as the metal gate of GaAs MOS devices to allow light illumination homogeneously on the whole gate area. In this way, LF *C-V* curves can be easily observed at relatively high frequencies under photoillumination. Semiconductor capacitance effect on GaAs is identified and used to explain the measured capacitance difference between hole accumulation (inversion) and electron inversion (accumulation). Due to the low density of states in GaAs, small semiconductor capacitance starts to be seriously detrimental to the gate capacitance when effective oxide thickness of high-*k* dielectric scales down to 1 nm.

The authors would like to thank M.A. Alam, K.K. Ng, S. Agarwal, A. Paul, and G. Klimeck for the valuable discussions. This work was supported by the National Science Foundation under Grant No. ECS-0621949 and the SRC FCRP MSD Focus Center.

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Citation: Applied Physics Letters **92**, 252105 (2008); doi: 10.1063/1.2953080
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